**USHA RAMA COLLEGE OF ENGINEERING AND TECHNOLOGY**

Department of Information Technology

**LESSON PLAN :: R-13**

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| **Academic Year** : 2016-17 | **Sem**  : I SEM |
| **Course**: Digital logic Design | |
| **Class** : II B.TECH | **Section** : I T |
| **Date of commencement of Class work** :13/6/2016 | **Date of end of Class work** : 09/10/2016 |
| **Prepared By**: Y V V N Vara Prasad | **Approved By**: HOD |

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| **S.No.** | **TOPIC** | **MODE OF DELIVERY** | **DATE** |
| **UNIT-I** | | | |
| **Number Systems** | | | |
| 1 | Binary, Octal, Decimal, Hexadecimal Number Systems | Lecture interspersed with discussion | 13/06/16 TO 14/06/16 |
| 2 | Conversion of Numbers From One Radix To Another Radix, | 15/06/16 TO  16/06/16 |
| 3 | r’s Complement and (r-1)’s Complement | 17/06/16 TO 18/06/16 |
| 4 | Subtraction of Unsigned Numbers, Problems | 19/06/16 TO 23/06/16 |
| 5 | Signed Binary Numbers | 24/06/16 TO 25/06/16 |
| 6 | Weighted and Non weighted codes | 27/06/16 TO 28/07/16 |
| 7 | Tutorial/Unit test | 29/07/16 |
| **UNIT-II** | | | |
| **Logic Gates And Boolean Algebra** | | | |
| 8 | Basic Gates NOT, AND, OR, Boolean Theorms | Lecture interspersed with discussion | 30/06/16 TO 01/07/16 |
| 9 | Complement And Dual of Logical Expressions | 02/07/16 TO 04/07/16 |
| 10 | Universal Gates, Ex-Or and Ex-Nor Gates | 05/07/16 TO 07/07/16 |
| 11 | SOP | 08/07/16 |
| 12 | POS | 10/07/16 |
| 13 | Minimizations of Logic Functions Using Boolean Theorems | 11/07/16 TO 12/07/16 |
| 14 | Two level Realization of Logic Functions Using Universal Gates | 13/07/16 TO 14/07/16 |
| 15 | Gate Level Minimization Karnaugh Map Method (K-Map) | 15/07/16 TO  19/07/16 |
| 16 | Minimization of Boolean Functions maximum up to Four Variables | 20/07/16 |
| 17 | POS and SOP | 21/07/16 |
| 18 | Simplifications With Don’t Care Conditions Using K-Map. | 22/07/16 |
| 19 | Tutorial/Unit test | 24/07/16 |
| **UNIT-III** | | | |
| **Combinational Logic Circuits** | | | |
| 20 | Design of Half Adder | Lecture interspersed with discussion | 24/07/16 |
| 21 | Full Adder | 26/07/16 |
| 22 | Half Subtractor, Full Subtractor | 27/07/16 |
| 23 | Ripple Adders and Subtractors | 28/07/16 |
| 24 | RippleAdder/Subtractor Using Ones and Twos Complement Method | 28/07/16 |
| 25 | Design of Decoders, Encoders, | 29/07/16 |
| 26 | Multiplexers,Demultiplexers | 30/07/16 |
| 27 | Higher Order Demultiplexers and Multiplexers | 01/08/16 |
| 28 | Priority Encoder | 02/08/16 |
| 29 | Code Converters, | 03/08/16 |
| 30 | Magnitude Comparator | 04/08/16 TO 05/08/16 |
| 31 | Tutorial/Unit test | 06/08/16 |
| **UNIT-IV** | | | |
| **Introduction to Sequential Logic Circuits** | | | |
| 32 | Classification of Sequential Circuits | Lecture interspersed with discussion | 16/08/16 TO 17/08/16 |
| 33 | Basic Sequential Logic Circuits : Latch and Flip-Flop | 18/08/16 TO 19/08/16 |
| 34 | RS- Latch UsingNAND and NOR Gates | 21/08/16 |
| 35 | Truth Tables | 22/08/16 |
| 36 | RS,JK,T and D Flip Flops | 23/08/16 TO 26/08/16 |
| 37 | Truth and Excitation Tables | 28/08/16 |
| 38 | Conversion of Flip Flops | 29/08/16 |
| 39 | Flip Flops With Asynchronous Inputs (Preset and Clear). | 30/08/16 |
| 40 | Tutorial/Unit test |  | 31/08/16 |
| **UNIT-V** | | | |
| **Registers and Counters** | | | |
| 41 | Design of Registers | Lecture interspersed with discussion | 01/09/16 TO 02/09/16 |
| 42 | Buffer Register, Control Buffer Registers | 04/09/16 TO  06/09/16 |
| 43 | Bidirectional Shift Registers | 07/09/16 |
| 44 | Universal Shift Register | 08/09/16 TO 09/09/16 |
| 45 | Design of Ripple Counters | 11/09/16 |
| 46 | Synchronous Counters and Variable Modulus Counters | 13/09/16 TO 15/09/16 |
| 47 | Ring Counter | 16/09/16 |
| 48 | Johnson Counter | 16/09/16 |
| 49 | Tutorial/Unit test |  | 18/09/16 |
| **UNIT-VI** | | | |
| **Introduction to Programmable Logic Device**s (PLOs) | | | |
| 50 | PLA | Lecture interspersed with discussion | 19/09/16 |
| 51 | PAL | 20/09/16 |
| 52 | PROM | 21/09/16 |
| 53 | Realization of Switching Functions Using PROM ,PAL and PLA | 22/09/16 TO 24/09/16 |
| 54 | Comparison of PLA,PAL and PROM. | 25/09/16 |
| 55 | Tutorial/Unit test | 26/09/16 |
| 56 | Revision Classes/ Subject |  | 27/09/16 TO  08/09/16 |

**\*I-MID 08/08/2016 TO 13/08/2016**

**\*II-MID 10/10/2016 TO 15/10/2016**

**TEXT BOOKS:**

1. Digital Design ,4/e, M.Morris Mano, Michael D Ciletti, PEA

2. Fundamentals of Logic Design, 5/e, Roth, Cengage

**REFERENCES:**

1. Switching and Finite Automata Theory,3/e,Kohavi, Jha, Cambridge.

2. Digital Logic Design, Leach, Malvino, Saha,TMH

3.Modern Digital Electronics, R.P. Jain, TMH

**List the Course Outcomes(Cos):**

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| Sub code | Sub Name | COs | Expected level of attainment  On 5 scale |
|  | Digital logic design | Understand the concepts of different logics and implementations  using Integrated circuits.  Design and analyze any Digital design in real time applications.  Extend the digital operations to any width by connecting the ICs and  can also design, simulate their results using hardware description  language.  Understand the concepts of MSI Registers and Modes of Operation  of Shift Registers, Universal Shift Registers.  . | 3.5  3.5  3.5  3.5 |

**SIGNATURE OF FACULTY SIGNATURE OF HOD**